Electronic Version
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Claims

[c1] bk2E001200406019What is claimed is:bk2E001200406019

1. A digital signal processor (DSP) for processing at least a digital data, the digital data having a plurality of representations, the representations including at least a fixed-point representation and a jumping floating-point representation, the DSP comprising:

a multiplication circuit for multiplying at least two short bit-length data together to generate a long bit-length digital data;

an extracting/shifting device electrically connected to the multiplication circuit for transforming a long bit-length digital data having the jumping floating-point representation into a long bit-length digital data having the fixed-point representation;

a plurality of representation converters, each of the representation converters transforming a specific digital data between the fixed-point representation and jumping floating-point representation through using a jumping floating-point arithmetic; and

an arithmetic unit for processing the digital data.

[c2] 2. The DSP of claim 1 further comprising a storage instrument electrically connected to the arithmetic unit for storing the digital data.

[c3] 3. The DSP of claim 1 wherein the jumping floating-point arithmetic is used for transforming a long bit-length digital data having the fixed-point representation into a short bit-length digital data having the jumping floating-point representation, or is used for transforming the short bit-length digital data having the jumping floating-point representation into the long bit-length digital data having the fixed-point representation.

[c4] 4. The DSP of claim 3 wherein the jumping floating-point arithmetic performs a magnifying shift to shift N bits of the long bit-length digital data having the jumping floating-point representation according to an absolute value of the long bit-length digital data wherein N is an integer not less than zero, eliminate a predetermined number of bits, and sets up a tail mark to generate the short bit-length digital data having the jumping floating-point representation.

[c5] 5. The DSP of claim 4 wherein a value of N varies in accordance with the absolute value of the long bit-length digital data, the value of N is reduced when the absolute value of the long bit-length digital data is increased, and

the value of N is increased when the absolute value of the long bit-length digital data is reduced.

[c6] 6. The DSP of claim 4 wherein the jumping floating-point arithmetic includes a plurality of displacement modes and each one corresponds to a different value of N.

[c7] 7. The DSP of claim 6 wherein each digital data comprises one sign bit, and a shifting mode and a value of N corresponding to the shifting mode are determined by comparing the sign bit with other bits of the long bit-length digital data.

[c8] 8. The DSP of claim 7 wherein the jumping floating-point arithmetic transforms the short bit-length digital data having the jumping floating-point arithmetic into the long bit-length digital data having the fixed-point arithmetic according to the tail mark and the sign bit.

[c9] 9. The DSP of claim 4 wherein when the two short bit-length digital data inputted into the multiplication circuit correspond to the jumping floating-point representation, the extracting/shifting device transforms the long bit-length digital data having the jumping floating-point representation into the long bit-length digital data having the fixed-point representation according to tail marks of the two short bit-length digital data having the

jumping floating-point representation.

[c10] 10. The DSP of claim 1 wherein the extracting/shifting device and the representation converters are electrically connected to at least an enabling control signal used for controlling if the extracting/shifting device and the representation converters are enabled.

[c11] 11. The DSP of claim 1 wherein the arithmetic unit is used for processing the digital data having the fixed-point representation.

[c12] 12. The DSP of claim 1 further comprising:
a data receiving end for receiving the digital data; and
a data writing-in end for storing a short bit-length digital data having the jumping floating-point representation into a memory device.

[c13] 13. A method applied to a digital signal processor (DSP) for transforming a long bit-length digital data having a fixed-point representation into a short bit-length digital data having a jumping floating-point representation, the method comprising:
(a) performing a magnifying shift to shift N bits of the long bit-length digital data having the fixed-point representation according to an absolute value of the long bit-length digital data, wherein N is an integer not less

than zero;

(b) eliminating a predetermined number of bits of the long bit-length digital data after step (a); and

(c) setting up a tail mark to generate the short bit-length digital data having the jumping floating-point representation after step (b), wherein the tail mark corresponds to a value of N.

[c14] 14. The method of claim 13 wherein the value of N is reduced when the absolute value of the long bit-length digital data is increased, and the value of N is increased when the absolute value of the long bit-length data is reduced.

[c15] 15. The method of claim 13 further comprising:

(d) in step (a), setting up a plurality of shifting modes, the shifting modes respectively correspond to different values of N;

(e) after step (d), determining a shifting mode and a corresponding value of N and performing a magnifying shift to shift N bits of the long bit-length digital data according to the absolute value of the long bit-length digital data;

(f) in step (c) and after step (e), setting up a tail mark corresponding to the shifting mode.

[c16] 16. The method of claim 15 wherein the long bit-length

digital data comprises a sign bit, and the shifting mode and the value of N corresponding to the shifting mode are determined by comparing the sign bit with other bits of the long bit-length digital data.

[c17] 17. The method of claim 16 wherein the short bit-length digital data comprises the tail mark, and the short bit-length digital data having the jumping floating-point representation is capable of being converted into the long bit-length digital data having the fixed-point representation according to the tail mark and the sign bit.

[c18] 18. The method of claim 13 further comprising:
(g) after step (c), storing the short bit-length digital data having the jumping floating-point representation into a memory device.

[c19] 19. A method applied to a digital signal processor (DSP) for transforming a short bit-length digital data having a jumping floating-point representation into a long bit-length digital data having a fixed-point representation, the short bit-length digital data having the jumping floating-point representation including a tail mark, the method comprising:
performing a minifying shift upon the short-bit digital data to shift N bits according to the tail mark, wherein N is an integer not less than zero; and

adding a predetermined number of bits to the short bit-length digital data.

[c20] 20. The method of claim 19 wherein the long bit-length digital data comprises a sign bit, and the method further comprising:
determining a value of each bit in N bits according to the sign bit; and
determining a value of each bit in the predetermined number of bits according to the sign bit.

[c21] 21. The method of claim 19 wherein the tail mark corresponds to a plurality of shifting modes, the shifting modes respectively correspond to different values of N, and the method further comprises determining a shifting mode and a corresponding value of N according to the tail mark.

[c22] 22. A digital signal processor (DSP) for processing at least a digital data, the digital data having a plurality of representations, the representations including at least a fixed-point representation and a jumping floating-point representation, the DSP comprising:
a data receiving end for receiving at least a short bit-length digital data;
a multiplication circuit electrically connected to the data receiving end for multiplying two short bit-length digital

data having the fixed-point representation to generate a long bit-length digital data having the fixed-point representation or multiplying two short bit-length digital data having the jumping floating-point representation to generate a long bit-length digital data having the jumping floating-point representation;

an extracting/shifting device electrically connected to the multiplication circuit for transforming a long bit-length digital data having the jumping floating-point representation into a long bit-length digital data having the fixed-point representation;

a first representation converter electrically connected to the data receiving end for transforming a short bit-length digital data having the jumping floating-point representation into a long bit-length digital data having the fixed-point representation or transforming a short bit-length digital data having the fixed-point representation into a long bit-length digital data having the fixed-point representation;

a multiplexing arithmetic module electrically connected to the first representation converter and the extracting/shifting device for performing selection and computation;

a storage instrument electrically connected to the multiplexing arithmetic module for storing at least a digital data processed by the multiplexing arithmetic module;

a second representation converter electrically connected to the storage instrument for transforming a long bit-length digital data having the fixed-point representation into a short bit-length digital data having the jumping floating-point representation; and
a data writing-in end for storing the short bit-length digital data having the jumping floating-point representation into a memory device.

[c23] 23. The DSP of claim 22 wherein each digital data comprises a sign bit.

[c24] 24. The DSP of claim 23 wherein each short bit-length digital data having the jumping floating-point representation comprises a tail mark.

[c25] 25. The DSP of claim 24 wherein the first representation converter transforms the short bit-length digital data having the jumping floating-point representation into the long bit-length digital data having the fixed-point representation according to the tail mark and the sign bit of the short bit-length digital data having the jumping floating-point representation.

[c26] 26. The DSP of claim 24 wherein the extracting/shifting device transforms the long bit-length digital data having the jumping floating-point representation into the long

bit-length digital data having the fixed-point representation according to the tail mark of the two short bit-length digital data having the jumping floating-point representation.

[c27] 27. The DSP of claim 22 wherein the second representation converter performs a magnifying shifting to shift N bits of the long bit-length digital data having the fixed-point representation wherein N is an integer not less than zero, eliminates a predetermined number of bits, and sets up a tail mark to generate the short bit-length digital data having the jumping floating-point representation.

[c28] 28. The DSP of claim 27 wherein a value of N varies in accordance with an absolute value of the long bit-length digital data, the value of N is reduced when the absolute value of the long bit-length digital data is increased, and the value of N is increased when the absolute value of the long bit-length digital data is reduced.

[c29] 29. The DSP of claim 22 wherein the extracting/shifting device, the first representation converter, and the second representation converter are electrically connected to at least an enabling control signal, and the enabling control signal is used for controlling if the extracting/shifting device, the first representation converter, and the second

representation converter are enabled.

[c30] 30. The DSP of claim 29 wherein the first representation converter transforms the short bit-length digital data having the jumping floating-point representation into the long bit-length digital data having the fixed-point representation when the enabling control signal enables the first representation converter, and the first representation converter transforms the short bit-length digital data having the fixed-point representation into the long bit-length digital data having the fixed-point representation when the enabling control signal disables the first representation converter.

[c31] 31. The DSP of claim 29 wherein the second representation converter transforms the long bit-length digital data having the fixed-point representation into the short bit-length digital data having the jumping floating-point representation when the enabling control signal enables the second representation converter, and the second representation converter transforms the long bit-length digital data having the fixed-point representation into the short bit-length digital data having the fixed-point representation when the second enabling control signal disables the second representation converter.

[c32] 32. The DSP of claim 22 wherein the multiplexing arith-

metic module is used for selecting and computing at least a long bit-length digital data having the fixed-point representation.

[c33] 33. The DSP of claim 22 wherein the representations further comprise an integer representation.